REMARKS

Currently pending claims 80-97 are for consideration by the Examiner.

The Examiner objected to the disclosure, alleging: "because of the following informalities: the phrase "07/02/99." (Amendment Al, line 2) should be change to --July 02, 1999, now US Patent No. 6,351,393.--." In response, Applicants have so changed the disclosure.

The Examiner rejected claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) as allegedly being anticipated by US Patent 4,882,454 to Peterson et al.

The Examiner rejected claims 81, 88, and 92 under 35 U.S.C. §103(a) as allegedly being unpatentable over Peterson et al.

The Examiner rejected claims 89 and 90 under 35 U.S.C. §103(a) as allegedly being unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeny et al.

Applicants respectfully traverse the §102 and §103 rejections with the following arguments.

35 U.S.C. §102(b)

The Examiner rejected claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) as allegedly being anticipated by US Patent 4,882,454 to Peterson et al.

The Examiner alleges: "Regarding claim 80, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102); positioning first (310) and second (311) dielectric layers on the thermally conductive layer; and position first (312) and second (313) pluralities of electrically conductive members on the first and second dielectric layers, each of said first and second pluralities of electrically conductive members adapted for having solder connection (103 and 104) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53)."

Applicants respectfully contend that Peterson does not anticipate claim 80, because Peterson does not teach each and every feature of claim 80. For example, Peterson does not teach "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate". The Examiner alleges that Peterson teaches "the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53)".

In response to the preceding argument by the Examiner, Applicants cite Peterson as

stating in col. 2, lines 44- 49 that "[i]deal performance in a surface mount application is achieved when CTE, thermal, weight and electrical properties are optimized by proper choice of materials and geometries. Core modifications can also be made to enhance thermal, CTE or weight properties when specific needs must be met. These involve the use of clad materials in the core, or composite cores of graphite, polymer, and copper." **The preceding disclosure in Peterson is non-specific** and therefore does not disclose specific features of claim 80. While Peterson discloses that optimization could be achieved by "proper choice of materials and geometries", Peterson does not state what is to be optimized and what choice of geometries could be utilized to achieve optimization. For example, Peterson does not specifically disclose optimization "**to substantially prevent failure of said solder connections** between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate" (emphasis added) as required by claim 80. As another example, Peterson does not specifically disclose "said thermally conductive layer being comprised of a material having a **selected thickness** and coefficient of thermal expansion to substantially prevent failure ..." (emphasis added) as required by claim 80.

Based on the preceding arguments, Applicants respectfully maintain that Peterson does not anticipate claim 80, and the claim 80 is in condition for allowance. Since claims 81-86 depend from claim 80, Applicants contend that claims 81-86 are likewise in condition for allowance.

Applicants respectfully contend that Peterson et al. does not anticipate claim 87, because

Peterson does not teach each and every feature of claim 87. For example, Peterson does not teach "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip". Applicants' arguments for claim 87 are the same as Applicants' arguments presented *supra* for claim 80. Based on the preceding arguments, Applicants respectfully maintain that does not anticipate claim 87, and the claim 87 is in condition for allowance. Since claims 88-90 depend from claim 87, Applicants contend that claims 88-90 are likewise in condition for allowance.

Applicants respectfully contend that Peterson et al. does not anticipate claim 91, because Peterson does not teach each and every feature of claim 91. For example, Peterson does not teach "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate". Applicants' arguments for claim 91 are the same as Applicants' arguments presented *supra* for claim 80. Based on the preceding arguments, Applicants respectfully maintain that does not anticipate claim 91, and the claim 91 is in condition for allowance. Since claims 92-97 depend from claim 91, Applicants contend that claims 92-97 are likewise in condition for allowance.

In the Examiner's "Response to Arguments", the Examiner alleges: "Peterson et al do teach the thermally conductive layer (102) being comprised of material having a selected

thickness and coefficient of thermal expansion (Col. 2, lines 44-47) to substantially prevent failure of the solder connections (103/104) between said first plurality of electrically conductive members and the semiconductor chip and between said second plurality of electrically conductive members and the circuit substrate" (Col. 1, lines 40-43)." In response, Applicants respectfully contend that col. 2, lines 44-47 of Peterson teaches selection of geometry without any disclosure of a selection of thickness. Applicants maintain that selection of geometry does not inherently imply a selection of thickness since geometry includes many attributes (thickness, linear dimensions other than thickness, areas, volumes, etc.). Additionally, col. 2, lines 44-47 of Peterson does not specifically or inherently identify the thermally conductive layer 102, and there are several structural portions (e.g., layers other than layer 102) in FIG. 1 of Peterson whose thickness and CTE may be controlled to substantially prevent failure of the solder connections. Applicants further maintain that col. 1, lines 40-43 of Peterson recites "[i]t is therefore an object of the invention to have a printed wiring board structure that possesses similar thermal expansion characteristics to surface mount components to be attached", which does not state anything about substantially preventing failure of the solder connections."

Also in the Examiner's "Response to Arguments", the Examiner alleges: "Applicants argue that Peterson et al do not specifically disclose the thickness and coefficient of thermal expansion of the core material is not persuasive. If the thermally conductive layer is provided such that it does not have a selected thickness and coefficient of thermal expansion, then Peterson et al teach (Cf. Col. 2, lines 17-19) that solder connection reliability will not be present." In response, Applicants respectfully contend that col. 2, lines 13-19 of Peterson teaches

"The elongated pads (103 and 104) along with the underlying vias (106 and 107) allow a spring action to be used to help absorb any difference in thermal expansion between the printed wiring board and the surface mount device. This greatly reduces the stress that is placed on the soldered connection and thus promotes reliability." Thus, Applicants respectfully contend that the Examiner's argument with respect to col. 2, lines 17-19 of Peterson is not persuasive because the reduction in stress on the solder connection is due to "the elongated pads (103 and 104) along with the underlying vias (106 and 107)" and not due to the thermally conductive layer.

Applicants respectfully contend that in order to support a rejection of a claim under 35 U.S.C. §102(b) through use of a reference, the Examiner must demonstrate that every feature of the claim is either expressly or inherently taught by the reference. Applicants respectfully contend that in order prove that a reference inherently teaches a feature, it is not sufficient to argue that the feature may be present or even that the feature probably is present. The Examiner must present an argument (e.g., a logical argument, an argument based on application of a physical law, etc.) that the feature **must** be present, which the Examiner has not done for the claims rejected under 35 U.S.C. §102(b). Instead, the Examiner has relied on conjecture and speculation.

The Examiner alleged that Applicants have waived patentability with respect to limitations recited in claims 82-86 and 93-97. In response, Applicants respectfully contend that the Examiner's allegation is without foundation and the Examiner has not cited any legally persuasive authority to support the Examiner's allegation. Furthermore, the Examiner's

allegation is in conflict with normal patent prosecution procedures regularly practiced by the United States Patent and Trademark Office.

Applicants contend that Applicants are in compliance with 37 CFR § 1.111(b) which states: "The reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references." Applicants contend that Applicants have presented arguments pointing out the specific distinctions believed to render the claims patentable over the references cited by the Examiner. With respect to claims 82-86 and 93-97, Applicants presented arguments in support of the patentability of independent claims 80 and 91, and such arguments also support the patentability of claims 82-86 and 93-97 which depend from claims 80 and 91, respectively and therefore include all of the limitations of claims 80 and 91, respectively. There is no legal authority that prevents Applicants from setting forth additional arguments in support of the patentability of claims 82-86 and 93-97 in a subsequent office action response or appeal.

35 U.S.C. §103(a)

The Examiner rejected claims 81, 88, and 92 under 35 U.S.C. §103(a) as allegedly being unpatentable over Peterson et al, and the Examiner rejected claims 89 and 90 under 35 U.S.C. §103(a) as being unpatentable over Peterson et al. in view of US Patent 5,691,041 to Frankeny et al. Since claim 81 depends from claim 80, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claim 81 is not unpatentable under 35 U.S.C. §103(a). Since claims 88-90 depends from claim 87, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claims 88-90 are not unpatentable under 35 U.S.C. §103(a). Since claim 92 depends from claim 91, which Applicants have argued *supra* to be patentable under 35 U.S.C. §102, Applicants maintain that claim 92 is not unpatentable under 35 U.S.C. §103(a).

The Examiner further alleged that Applicants have waived patentability for claims 89-90 with respect to the combinability of the teachings of Peterson et al. and Frankeny et al. In response, Applicants respectfully contend that the Examiner has not cited any legally persuasive authority to support the Examiner's allegation. Furthermore, the Examiner's allegation is in conflict with normal patent prosecution procedures regularly practiced by the United States Patent and Trademark Office.

Applicants contend that Applicants are in compliance with 37 CFR § 1.111(b) which states: "The reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references." Applicants contend that Applicants have presented arguments pointing out the specific

distinctions believed to render the claims patentable over the references cited by the Examiner. With respect to claims 89-90, Applicants presented arguments in support of the patentability of independent claim 87, and such arguments also support the patentability of claims 89-90 which depend from claim 87 and therefore include all of the limitations of claim 87. There is no legal authority that prevents Applicants from setting forth additional arguments in support of the patentability of claims 89-90 in a subsequent office action response or appeal.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 80-97 and the entire application meet the acceptance criteria for allowance, and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact Applicants' representative at the telephone number listed below.

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